UNITED STATES PATENT APPLICATION

FOR

CAPACITANCE MEASUREMENTS
FOR AN INTEGRATED CIRCUIT

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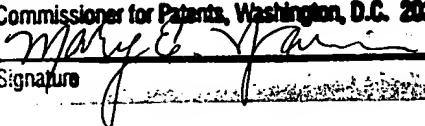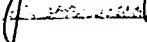
CAPACITANCE MEASUREMENTS
FOR AN INTEGRATED CIRCUIT

FIELD OF THE INVENTION

The invention relates to circuit design parameter measurement. More particularly,

5   the invention relates to a method and apparatus for high precision measurement of cross

coupling and total capacitance of wires on an integrated circuit design.

BACKGROUND OF THE INVENTION

Until the advent of deep sub micron integrated circuit processes, timing behavior

of integrated circuits has been dictated by transistor considerations, mostly transistor

10   travel time and the number of logic levels a signal traverses during a clock cycle.

Accurate models of transistor device parameters were the key element for the prediction

of circuit timing behavior.

For feature sizes larger than 0.35 μm wire delay is typically less than 20% of total

timing delay. To account for the 20% contribution to total timing delay high precision

15   delay estimates were not required for wire delay. A relatively large (e.g., 25%)

uncertainty in extracting resistance and/or capacitance values results in approximately a

4% overall error in time delay modeling.

Computer aided design (CAD) programs used for integrated circuit design used

simplified models to compute wire delay from resistance and capacitance data extracted

20   using a layout database. Resistance and capacitance models that provide less than 25%

uncertainty are well known in the art. For example, resistance estimates can be generated

based on the geometric shape of the line to be estimated. Capacitance estimates can be

generated based on a parallel plate capacitor model with perimeter fringe contribution

corrections. These modeling approaches are useful for integrated circuit designs having

device sizes greater than 0.35 μm.

However, as device sizes decrease the relative importance of wire delay increases.

5   Wire extraction programs can be calibrated with accurate measurements of capacitance.

One approach to accurate wire capacitance measurement is provided by B.W. McGaughy,

J.C. Chen, D. Sylvester and C. Hu "A Simple Method for On-Chip Sub-Femto Farad

Interconnect Capacitance Measurement," IEEE Electron. Device Letters, Vol. 18, No. 1,

pp. 21-23, January 1997, (hereinafter referred to as "the IEEE paper"), which discloses a

10   method for determining cross coupling capacitance. However, the method described in

the IEEE paper suffers shortcomings that are explained in detail in a white paper by J. C.

Chen and Roberto Suaya entitled "Proper On-Chip Capacitance Measurement,"

(hereinafter referred to as "the white paper"). A brief overview of the white paper is

provided below.

15   Figure 1 represents the circuit used in the IEEE paper to measure cross coupling

capacitance. A general method to measure capacitance consists of measuring the total

charge deposited on the capacitor, which can be accomplished by measuring DC currents,

frequency of applied signals, and voltage. The following formula permits the

determination of capacitance:

20    $I = CV_{dd}f$ (Equation 1)

where I is a dc current reading, C is a load capacitance, V_{dd} is the voltage supply level,

and f is the frequency of the waveforms applied.

The voltage waveform of **Figure 2** used in the IEEE paper are non-overlapping waveforms that provide, except for leakage, no current path between V_{dd} and ground in the circuit of Figure 1. In the IEEE paper, the unknown capacitance is measured as the difference between two current readings on the two current meters in Figure 1. The

5   process is flawed because of charge redistribution. The capacitance coupling between two structures, depends on the presence of other nearby structures.

Consider in Figure 1, two identical load structures, C and C'. The capacitance of C to ground on the left side of the structure is different from the capacitance C' to ground on the right side. The difference is due to the redistribution of the electric field due to the

10   presence of the second conductor. The capacitance difference can be quite large.

Configurations like the one shown in **Figure 3**, where the load wire and its neighbors are on the same physical layer and are separated by minimum distance, constitute a case where the direct application of the method of the IEEE paper would result in up to 70% error in the extraction of the unknown cross coupling capacitance.

15   There is, in addition, the uncertainty related to the lack of equality in the capacitance of the transistors on the two sides of the mirror structure. This additional source of error becomes more significant as the device size decreases.

SUMMARY OF THE INVENTION

A method and apparatus for determining cross coupling capacitance of wires in an integrated circuit. A first predetermined signal is applied to a first wire. A second predetermined signal is applied to a second wire that is parallel to the first wire. A cross coupling capacitance between the first wire and the second wire is determined based, at least in part, on a current signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated by way of example, and not by way of limitation in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

5   **Figure 1** is a prior art circuit for use in measuring cross coupling capacitance.

Figure 2 is a voltage waveform for use to measure the capacitance of the circuit of Figure 1.

Figure 3 is a prior art circuit for measuring cross coupling capacitance between parallel wires on the same layer that leads to large errors.

10   **Figure 4** is a circuit suitable for use in determining cross coupling capacitance according to one embodiment of the invention.

Figure 5 is a voltage waveform for use in measuring the cross coupling capacitance of the circuit of Figure 4 according to one embodiment of the invention.

Figure 6 is an equivalent circuit diagram corresponding to the circuit of Figure 4.

15   **Figure 7** is one among the multiple extensions of the measuring device method shown in Figure 4 to multiple wire configurations.

Figure 8 is a block diagram illustrating an overview of an IC design simulation tool.

Figure 9 is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention.

Figure 10 is one embodiment of a computer system suitable for use with the invention.

DETAILED DESCRIPTION

In the following description, for purposes of explanation, numerous specific

details are set forth in order to provide a thorough understanding of the invention. It will

be apparent, however, to one skilled in the art that the invention can be practiced without

5   these specific details. In other instances, structures and devices are shown in block

diagram form in order to avoid obscuring the invention.

Reference in the specification to "one embodiment" or "an embodiment" means

that a particular feature, structure, or characteristic described in connection with the

embodiment is included in at least one embodiment of the invention. The appearances of

10   the phrase "in one embodiment" in various places in the specification are not necessarily

all referring to the same embodiment.

The invention provides a method and apparatus for determining cross coupling

capacitance of wires in an integrated circuit, total capacitance can be determined by

adding the different cross coupling capacitance. The capacitance information derived

15   according to the invention can be used, for example, to calibrate a parasitic extraction

engine or to calibrate an integrated circuit fabrication process. The capacitance

information can also be used to improve timing and noise simulations of circuits

particularly for deep sub-micron circuits since wire capacitance effects play a dominant

role for deep submicron circuits.

20   Briefly, the invention allows the measurement of cross coupling capacitance

between two lines by applying predetermined voltage signals to specific circuit elements.

The resulting current allows for simple computation of cross coupling capacitance, and

total capacitance by addition. The capacitance values obtained can then be used to

calibrate extraction engines, processes, and provide input to timing and noise simulators.

Figure 4 is a circuit suitable for use in determining cross coupling capacitance

according to one embodiment of the invention. The circuit of Figure 4 removes transistor

5   mismatch and charge redistribution errors, which improves the accuracy of measurement

as compared to Figures 1 and 3 above.

The main structure of Figure 4 includes ammeter 400, transistor 410, transistor

420 and a minimum size structure that connects load wire 440 with the main structure. In

the example of Figure 4, load wire 440 and neighbor wire 450 are on the Metal2 layer;

10   however, Metal2 layer wires are not required. In the embodiment of Figure 4, load wire

440 is coupled to the main structure by Metal1-via-Metal2 structure 435 and wire 430.

The circuit of Figure 4 is used to measure cross coupling capacitance between

wire 440 and wire 450, Wire 440 is parallel to wire 450. Inverter 460 is coupled to wire

450 by wire 455. In one embodiment, inverter 460 is far enough away from the main

15   structure to reduce noise input on wire 400.

Figure 5 is a voltage waveform for use in measuring the cross coupling

capacitance of the circuit of Figure 4 according to one embodiment of the invention.

Voltage V_1 is applied to the gate of transistor 420. Voltage V_2 is applied to the gate of

transistor 410. Voltage V_3 is input to inverter 460. Referring back to Figure 4, only the

20   portion of the line (i.e., wire 450 and 455) driven by V_3 (i.e., wire 450) gives an

appreciable contribution to the cross coupling capacitance affecting line segment 440.

Capacitance measuring for the circuit of Figure 4 using the voltage waveforms of Figure

5 are described below.

Figure 6 is an equivalent circuit diagram corresponding to the circuit of Figure 4.

With reference to the circuit of Figure 6, the following name convention applies: C_1, C_2, C_{line}, and $C_{coupling}$ refer, respectively, to transistor plus Metal1-via-Metal2 minimum structure and other parasitic capacitances to ground, Metal2 ground capacitance, total

5   capacitance of nearest neighbor, and the capacitance coupling between wires **440 and**

450.

Before applying the voltage waveforms of Figure 5, the voltage applied to the external inverter 460, $V_3 = V_{dd}$. (or ground). Ammeter 400 is used to measure the charge, Q, that flows into node 600 of Figure 6. Node 600 gets charged when $V_2 = V_1 = 0$, and this charge is equal to:

$$Q = I / f = (C_1 + C_2 + C_{coupling})V_{dd} \qquad \text{(Equation 2)}$$

The measurement proceeds by applying for a sufficiently large number of cycles a periodic signal to V_3, having the same frequency as the signal applied to V_1, V_2. The relative rise and fall times of the external signals do not matter.

15   Following the discharge to ground of transistor 420, V_3 is switched to ground, and $C_{coupling}$ is charged to V_{dd}. This charge redistributes among the capacitors because node 600 is in a high impedance state. The intermediate voltage at node 600 is not important, provided that the switching of transistors 420 and 410 is not altered. Next, V_2 is switched to ground and

20   $$Q' = (C_1 + C_2)V_{dd} \qquad \text{(Equation 3)}$$

flows into node 600. The difference between the direct current readings represented by Equations 2 and 3, (when $V_3 = V_{dd}$, on static mode, and when $V_3 = 0$ on periodic mode) normalized to V_{dd} identifies $C_{coupling}$.

$$C_{coupling} = (Q - Q')/V_{dd} \qquad \text{(Equation 4)}$$

5   The measurement of $C_{coupling}$ in the circuit of Figure 4 (represented by an equivalent circuit in Figure 6) is free of transistor capacitance influence and insensitive to charge redistribution errors, as compared to the dual mirror structured circuits described in the IEEE paper. However, errors due to a minimum size probe reaching the Metal2 configuration and errors arising from coupling to the orthogonal portion of the aggressor

10   wire to the wire under test remain. In one embodiment, for a 0.25 μm process with SiO dielectric, the error bound is 0.02 fF. The magnitude of this error decreases with scaling and lower permitivity dielectric materials. Thus, the measurement described with respect to Figures 4-6 allows highly accurate measurement of cross coupling capacitance.

In an alternative embodiment, ammeter 400 can be placed between the source of

15   transistor 420 and ground. This alternative embodiment provides the same accuracy and the embodiments described with respect to Figures 4-6.

The measurement technique described with respect to Figures 4-6 is based on static charge measurement. To the extent that the dielectric constant of the medium is frequency independent, the total deposited charge is frequency independent. Statistical

20   error can be made negligible by performing multiple charge measurements at the same and different frequencies, or alternatively, measuring the slope of the charge as a function

of V_{dd}. Both techniques provide a $\sqrt{n}$ improvement in the statistical error, where n is the number of measurements.

The technique of the invention provides improved calibration of several capacitance elements with a single structure because the technique is extensible to

5   simultaneous and non simultaneous switching of multiple neighbors. The timing scheme is similar to the single wire case, with the addition of another voltage signal V_4 feeding via another inverter the second neighbor wire. There are two choices for the timing of V_4: 1) $V_3 = V_4$, the simultaneous switching of the two wires (in this case, the two neighbor wires are identical, and $2C_{coupling}$ is determined thereby halving the absolute error on

10   $C_{coupling}$); or 2)the central wire to the two neighbor wires are determined independently with the same library element, thereby saving valuable space on the silicon chip (V_4 has the same sequencing as V_3, except that $V_4 = V_{dd}$ while V_3 is periodic).

The neighbors can be on different metal layers. For example, a general nearest neighbor configuration can consist of nine wires on three metal layers, where, with one

15   library element one can measure all the couplings from the middle wire in the middle layer to each of its neighbors. There are eight couplings that can be measured with one library element via a direct extension of the last procedure. The overall configuration consists of two V_{dd} lines, one common ground line, two voltages feeding, the N and P transistors of the measuring device and eight voltages feeding the eight nearest neighbor

20   wires. The reason for two V_{dd} lines is to separate the V_{dd} for the measuring structure from the V_{dd} feeding the eight inverters, to reduce noise.

This last technique is particularly useful for library validation. Library validation is the process of building sufficient structures to be measured within the same integrated

circuit chip to characterize a design. Typically, these libraries can be large but kept reasonably small with non simultaneous switching, as described above. The technique of the invention can also be used to optimize process parameters based on wire timing considerations.

5   **Figure 8** is a block diagram illustrating an overview of an IC design simulation tool. As illustrated, IC design simulation tool 800 is constituted with design reader 802, static partitioner 803 and simulation engine 804 comprising dynamic partitioner 807, scheduler 809, node evaluator 808 and model evaluators 806. The elements are operatively coupled to each other as shown. Design reader 802 and some model

10   evaluators 806, in particular a transistor model evaluator and a wire model evaluator, are incorporated with the teachings of the present invention. Certain aspects of static partitioner 803, dynamic partitioner 807 and scheduler 809 are the subject of co-pending U.S. Patent application number 09/333,124, filed June 14, 1999, and entitled "CIRCUIT SIMULATION USING DYNAMIC PARTITION AND ON-DEMAND EVALUATION"

15   which is hereby fully incorporated by reference.

In one embodiment, the model evaluators evaluate transistor models and wire models having capacitance determined as described above. The capacitance information, both cross-coupling capacitance and total capacitance, can be combined with other device modeling information to provide accurate models and evaluations of the models.

20   Design reader 802 is used to read design description 810 provided by a designer. Design description 810 includes connectivity information connecting various models modeling electronic devices in the IC design. In one embodiment, in addition to flattening a hierarchical design, design reader 802, also assigns device characterizations

to selected ones of the electronic devices of the IC design. In one embodiment the device characterizations are determined as described above. Static partitioner 803 pre-compiles or pre-partitions the IC design into static partitions as well as pre-processes the static partitions into a form particularly suitable for the dynamic partitioner 807.

5   During simulation, dynamic partitioner 807 further forms and re-forms dynamic partitions of the IC design that are relevant, referencing the pre-formed static partitions. Scheduler 809 determines whether evaluations are necessary for the dynamic partitions for the particular simulation time step, and schedules the dynamic partitions for evaluation on an as-needed or on-demand basis. Accordingly, node evaluator 808 and

10   model evaluators 806 are selectively invoked on an as needed or on-demand basis to evaluate the states of the connections connecting the models, and various parameter values of the models, such as current, voltage and so forth, respectively.

In one embodiment, at least one of the model evaluators adaptively performs the model evaluations at different accuracy or performance levels in accordance with the

15   assigned device characterizations of the devices. Where accuracy is needed, the evaluations are performed through matrix solution. Formation of static partitions, and formation of dynamic partitions as well as scheduling evaluations on demand, i.e. on an as needed basis are explained in the above identified incorporated by reference co-pending U.S. patent applications. Further detail with respect to circuit simulation is

20   provided in and co-pending U.S. Patent application number 09/333,122, filed June 14, 1999, and entitled "ADAPTIVE INTEGRATED CIRCUIT DESIGN SIMULATION TRANSISOR MODELING AND EVALUATION," which is hereby incorporated by reference.

Figure 9 is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention. As illustrated, the present invention includes parasitic extraction tool (PEX) 902 and parasitic database (PDB) 904. PEX 902 generates electrical modeling data for layout nets of an IC design, e.g. a deep sub-micron IC design, and stores the generated electrical modeling data in PDB 904 for use by client applications, such as post layout analysis applications 918. Examples of post-layout analysis applications 918 include Delay Calculator by Ultima Technology of Sunnyvale, CA, and Path Mill and Time Mill by Synopsis Inc. of Mountain View, CA.

PEX 902 generates the electrical modeling data for the layout nets using extracted connectivity and geometrical data of the layout nets. In one embodiment PEX 902 generates capacitive modeling data as described above. As shown, PEX 902 includes read function 906 that operates to input these connectivity and geometrical data of the layout nets. For the illustrated embodiment, the extracted connectivity and geometrical data of the layout nets are input from filtered databases (FDB) 916.

The extracted connectivity and geometrical data are stored in FDB 916 by layout cell hierarchies, one FDB per layout cell hierarchy, and indexed by layout nets. The connectivity and geometrical data were extracted at least in part in accordance with specified parasitic effect windows of the various layers of the IC design. Read function 906 operates to retrieve the connectivity and geometrical data of the layout nets from FDB 916 using the stored layout net indices. FDB 916 is the subject of co-pending U.S. Patent application number 09/052,895, filed March 31, 1998, and entitled "METHOD AND APPARATUS FOR EXTRACTING AND STORING CONNECTIVITY AND GEOMETRICAL DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT

DESIGN," which is assigned to the corporate assignee of the present invention. The co-pending application is hereby fully incorporated by reference.

PDB 904 is designed to accommodate a large volume of electrical modeling data and concurrent accesses by multiple client applications, which is typically of today's and

5   future deep sub-micron IC designs and design environments. For the illustrated embodiment, PDB 904 has physical organization 914 that allows a large volume of electrical modeling data to be stored in multiple physical media, and application interface 910 that shields physical organization 914 from PDB users, e.g. PEX 902 and post layout analysis applications 918. Additionally, PDB 902 has logical organization 912 that

10   abstracts physical organization 914 to facilitate implementation of application interface 910.

For the illustrated embodiment, PEX 902 includes write function 908 that operates to store the generated electrical modeling data of the layout nets into PDB 904 using application interface 910. In alternate embodiments, write function 908 may store

15   the generated electrical modeling data of the layout nets using either logical and/or physical organizations 912-914. Similarly, selected ones of the client applications, e.g. post-layout analysis applications 918, may also elect to access PDB 904 through logical and/or physical organizations 912-914.

Read function 906 and write function 908 are the subject of co-pending U.S.

20   Patent application number 09/052,915, filed March 31, 1998 and entitled "METHOD AND APARATUS FOR GENERATING AND MAINTAINING ELECTRICAL MODELING DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT DESIGN," which is assigned to the corporate assignee of the present invention. The co-

pending application is hereby fully incorporated by reference. Except for read function

906 and write function 908, PEX 902 is intended to represent a broad category of

electrical modeling tools known in the art. Examples of these electrical modeling tools

include but not limited to Pattern Engine of xCalibre by Mentor Graphics, Columbus by

5   Frequency Technology of San Jose, CA, and Arcadia by Synopsis.

Figure 10 is one embodiment of a computer system suitable for use with the

invention. Computer system 1000 can be used, for example, for extraction and/or modeling

of integrated circuits using the teachings of the present invention. Computer system 1000

includes bus 1001 or other communication device to communicate information and

10   processor 1002 coupled to bus 1001 to process information. While computer system 1000

is illustrated with a single processor, computer system 100 can include multiple processors

and/or co-processors. Computer system 1000 further includes random access memory

(RAM) or other dynamic storage device 1004 (referred to as main memory), coupled to bus

1001 to store information and instructions to be executed by processor 1002. Main

15   memory 1004 also can be used to store temporary variables or other intermediate

information during execution of instructions by processor 1002.

Computer system 1000 also includes read only memory (ROM) and/or other static

storage device 1006 coupled to bus 1001 to store static information and instructions for

processor 1002. Data storage device 1007 is coupled to bus 1001 to store information and

20   instructions. Data storage device 1007 such as a magnetic disk or optical disc and

corresponding drive can be coupled to computer system 1000.

Computer system 100 can also be coupled via bus 1001 to display device 1021,

such as a cathode ray tube (CRT) or liquid crystal display (LCD), to display information to

a computer user. Alphanumeric input device 1022, including alphanumeric and other keys, is typically coupled to bus 1001 to communicate information and command selections to processor 1002. Another type of user input device is cursor control 1023, such as a mouse, a trackball, or cursor direction keys to communicate direction information and command

5   selections to processor 1002 and to control cursor movement on display 1021.

According to one embodiment, extraction and/or modeling can be performed by computer system 1000 in response to processor 1002 executing sequences of instructions contained in main memory 1004. Instructions are provided to main memory 1004 from a storage device, such as magnetic disk, a read-only memory (ROM) integrated circuit (IC),

10   CD-ROM, DVD, via a remote connection (e.g., over a network), etc. In alternative embodiments, hard-wired circuitry can be used in place of or in combination with software instructions to implement the present invention. Thus, the present invention is not limited to any specific combination of hardware circuitry and software instructions.

In the foregoing specification, the invention has been described with reference to

15   specific embodiments thereof (the measurement of a Metal2 wire capacitance coupling to another Metal2 wire). It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

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